Integrated Passive Components for On-chip Power Conversion

Gregory W. Donohoe, Ph.D., P.E.
gdonohoe@uidaho.edu
(208) 885-6501

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PI: Gregory W. Donohoe
Computer Science Department
University of Idaho
JEB 237, PBO 441010
Moscow, ID 83844-1010
gdonohoe@uidaho.edu

To: Glenn Forman
G.E. Global Research
1 Research Circle, Bldg K-1 3C39A
Niskayuna, NY 12309
(518) 387-7420
formanga@research.ge.com

Contract: GE PO Number/Release 400070053

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Executive Summary

This project constitutes exploratory research to investigate fabricating passive components – inductors, capacitors, and resistors – onto CMOS integrated circuits. To give the project focus, the scope is targeted to a specific application: performing power regulation directly on digital Ultra Low Power (ULP) microchips, to provide stable power for the digital circuits. In the effort to reduce power consumption, CMOS supply voltages have been decreasing over the years toward 0.5V. Providing stable $\frac{1}{2}$ V DC power across a subsystem is a major challenge. The approach chosen here is to place voltage conversion regulation circuits on the die that hosts the digital load, and therefore on the die side of distributed series inductances. The American Semiconductor Flexfet™ SOI CMOS process was chosen as the target semiconductor platform technology. The key technology barriers are power regulation circuits that are compatible with a CMOS process, and the need for high-quality on-chip passive components, along with the required circuits and fabrication processes.

Desired Benefits

1. Improved power delivery to the chip for low-power operation.
2. Reduced size of electronic systems by eliminating external passives.
3. Improved performance, bypassing the wires and metal traces that degrade operating speed.
4. Reconfigurability: the ability to rewire their internal structures to optimize the chip for a particular task, after it is fabricated.

Key Participants

University of Idaho
- Dr. Gregory W. Donohoe, PI, Computer Science. Project lead.
- Dr. Herbert Hess, Co-I, Electrical and Computer Engineering. Integrated Power Circuits
- Dr. Daniel Choi, Co-I, Materials Science and Engineering, Capacitors

Boise State University
- Dr. Kris Campbell, College of Engineering. Programmable resistors.

American Semiconductor, Inc., Boise, ID
- Dale Wilson, Project Lead. Engineering support, test chip fabrication.

Brief Overview

This is the second phase of a three-phase project. The first phase was funded in FY07-08. The second phase began in January 2011. The third phase is in the proposal stage. The sponsor is the Air Force Research Laboratory, Space Protection/Electronics Branch, Kirtland AFB, NM.
The day-to-day documentation of the project is maintained on a wiki at:


This includes the project overview and more detailed background, including documentation of Phase 1.

Phase 1 Results

1. ULP Digital Load. A processing element design taken from the experimental Field Programmable Processor Array chip was designed for the American Semiconductor Flexfet process, including connections to the Flexfet “back gate”, enabling the switching threshold to be adjusted electrically. This is the basis of the ULP test load. Test chips were fabricated, and are being tested at Bucknell University.

2. Power circuits. Three different power circuit topologies were designed, and test chips were fabricated on the Flexfet SOI CMOS process. These were tested, and laid the groundwork for a second round of power circuits.

3. Inductors. (This work was performed at the University of Alabama, not on contract for Phase 2.) A family of ferrite-clad spiral inductors was designed and fabricated. Ferrite cladding increased inductance per unit area by approximately 20% over air-core inductors, and more than doubled the Q factor.

Fabrication Methods

a. Ferrite cladding was deposited onto inductors by sputtering

b. Ferrite cladding was deposited onto inductors by low-temperature electrophoretic deposition.

c. Inductor thin films with controllable resistance were demonstrated using a low-temperature accelerated nanoparticle technique. This film was not applied to inductors.

4. Programmable Resistors. Chalcogenide-based programmable resistors were developed, fabricated, packaged, and demonstrated in circuits.

Phase 2 Tasks

1. Power circuits. Lead: H. Hess
2. Capacitors. Lead: D. Choi
3. Programmable resistors. Lead: K. Campbell
Results for Reporting Period

Power Circuits (H. Hess)

Test Chip

Tested the full buck converter from the test chip. Used a static load. Operated the circuit from near DC to 5 MHz.

Getting an output that matches simulation, except there is more transient switching noise in the test chip than in the simulation, due to parasitic inductances and capacitances. Switching noise is lower than that scene in similar circuits implemented on printed circuit boards. We attribute that to reduced parasitic inductance of on-chip connections as opposed to PCB wiring.

Complete test results will be presented in the final report.

Capacitors (D. Choi)

Staffing (updated)

Capacitors (D. Choi)

- Ke Xu, M.S. Student, Materials Science and Engineering (financially supported by other project)

Phase 2 Work Plan & Achievements

- Design of 'Energy harvest module for on-chip capacitor incorporated with RFID'. The capacitor is used for charging and discharging the electrical charge. When the electromagnetic field is applied by RF reader, the electromagnetic field is received by the antenna and stored the electrical charges in the capacitor on the RFID tag. The electrical discharging rate can be controlled by the applied frequency from the RF reader as shown in Fig 1.
Figure 1. The schematic diagram of RFID module attached on the on-chip capacitor.

- Simulation work on the on-chip capacitor based on a vertical array of silver (Ag) nanowires (NWs) as electrodes and Bismuth-Ferric-Oxides (BFO) as a dielectric material: In progress
  - Optimizing design of the capacitor to maximize capacitance

- Developing a low-cost process for fabricating Ag NWs as high surface area and high electrically conductive electrodes for the on-chip capacitors: In progress
  - Process control of electrodeposition of Ag thin-films (top electrodes)

- Simulation of MEMS "Swiss-roll" type on-chip capacitor based on Ag nanowires as electrodes: In progress

Activities for Next Reporting Period

Designing next test chip with a complete boost converter, to be fabricated in a TSMC 0.18 micron mixed signal process. This will use an on-chip inductor.
Programmatic Issues

The possibility of missing circuits on the test chips, reported previously, has been resolved. There were no missing circuits; there was a communication breakdown between the vendor and the design team.

Inventions Reported

None.

Publications, Presentations, Proposals, Awards

Follow-On Proposals

- "Development of Integrated Passive Electronic Components for AHST and Other Space Applications" with American Semiconductors (Boise, ID), Notice of Intent for NASA EPSCoR program.

- Proposal for National Science Foundation Electronics, Photonics and Magnetic Devices (EPMD) program: Drafting in progress

Presentations

- Daniel Choi, "On-chip capacitor for Power IC applications", Innovative Technology Section of Intel Corporation on August 16th, 2012

Theses and Dissertations